IN THE CLAIMS:

1-54. (Cancelled).

55. (Previously Presented) A device for transporting integrated circuit chips and for testing said integrated circuit chips during said transporting, said device comprising:

an in-transit box adapted to transport said integrated circuit chips;

a plurality of test boxes mounted in said in-transit box;

a plurality of test boards mounted in each one of said test boxes and adapted to test said integrated circuit chips during said transporting of said integrated circuit chips; and

a power supply in each of said test boxes, connected to each of said test boards, and adapted to supply power to said test boards during said transporting and said testing of said integrated circuit chips,

wherein each of said test boards comprises:

multiple sockets adapted to hold and electrically connect to multiple integrated circuit chips; and

testing circuitry electrically connected to said sockets for testing said multiple integrated circuit chips.

56. (Currently Amended) The device in claim 55, all the limitations of which are incorporated herein by reference, wherein each of said test boards includes visual test failure indicators, such that one of said visual test failure indicators is adjacent each of said sockets.

57. (Currently Amended) The device in claim 55, all the limitations of which are incorporated herein by reference, wherein for each test box said power supply comprises a power bus electrically connected between said test boards and one of a battery in said test box and a separate power supply in said in-transit box.

58. (Currently Amended) The device in claim 55, all the limitations of which are incorporated herein by reference, wherein each of said test boards includes a memory adapted to store test results.

59. (Currently Amended) The device in claim 55, all the limitations of which are incorporated herein by reference, wherein each of said test boards includes a known good integrated circuit chip.

60. (Currently Amended) The device in claim 59, all the limitations of which are incorporated herein by reference, wherein each of said test boards includes comparators electrically connected to said sockets.

61. (Currently Amended) The device in claim 60, all the limitations of which are incorporated herein by reference, wherein said testing circuitry is adapted to supply identical test patterns to said integrated circuit chips to be tested and to said known good integrated circuit chip, and

wherein said comparators compare an output generated by said known good integrated circuit chip with outputs generated by said integrated circuit chips to be tested to identify defective integrated circuit chips.

62. (Currently Amended) The device in claim 61, all the limitations of which are incorporated herein by reference, wherein said comparators are in parallel to one another such that all comparisons performed by said comparators are made simultaneously.

63. (Previously Presented) A device for transporting application specific integrated circuit (ASIC) chips and for testing said application specific integrated circuit (ASIC) chips during said transporting, said device comprising:

an in-transit box adapted to transport ASIC chips;

a plurality of test boxes mounted in said in-transit box;

a plurality of test boards mounted in each one of said test boxes and adapted to test said ASIC chips during said transporting of said ASIC chips; and

a power supply in each of said test boxes, connected to each of said test boards, and adapted to supply power to said test boards during said transporting and said testing of said ASIC chips,

wherein each of said test boards comprises:

multiple sockets adapted to hold and electrically connect to multiple ASIC chips; and

testing circuitry electrically connected to said sockets for testing said multiple ASIC chips, wherein said testing circuitry includes comparators arranged in parallel and electrically connected to said sockets, such that said testing circuitry tests all of said multiple ASIC chips simultaneously, and

wherein said testing circuitry identifies a defective ASIC chip as one having a different output when compared to outputs of the other ASIC chips, when all of said multiple ASIC chips are supplied with identical inputs.

64. (Currently Amended) The device in claim, 63 all the limitations of which are incorporated herein by reference, wherein all of said multiple ASIC chips have an identical design.

65. (Currently Amended) The device in claim 63, all the limitations of which are incorporated herein by reference, wherein each of said test boards includes visual test failure indicators, such that one of said visual test failure indicators is adjacent each of said sockets.

66. (Currently Amended) The device in claim 63, all the limitations of which are incorporated herein by reference, wherein for each test box said power supply comprises a power bus electrically connected between said test boards and one of a battery in said test box and a separate power supply in said in-transit box.

67. (Currently Amended) The device in claim 63, all the limitations of which are incorporated herein by reference, wherein each of said test boards includes a memory adapted to store test results.

68. (Currently Amended) The device in claim 63, all the limitations of which are incorporated herein by reference, wherein each of said test boards includes a known good integrated circuit chip.

69. (Currently Amended) The device in claim 68, all the limitations of which are incorporated herein by reference, wherein all of said comparators are connected to said known good integrated circuit chip such that any ASIC chips that produce an output different than the output produced by said known good integrated circuit chip is identified as a defective ASIC chip.

70. (Currently Amended) The device in claim 63, all the limitations of which are incorporated herein by reference, wherein by comparing whether outputs of all ASIC chips are identical, said testing circuitry does not require a specific proper output that a given input should produce for the specific design of ASIC chip being tested.

71-104 (Cancelled).